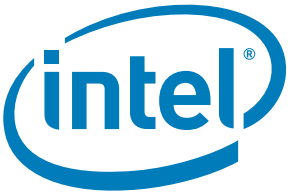

Intel® 3100 Chipset

Specification Update

November 2007

Notice: The Intel® 3100 Chipset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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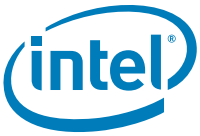
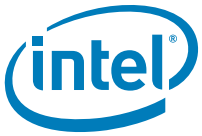
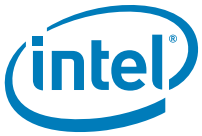




Contents

Revision History

Revision	Description	Date
001	Initial public release	June 2006
002	Added A1 information (i.e. device id, component markings, fixed errata #35-37), added specification clarifications #2-3, added documentation change #1.	November 2006
003	Corrected inaccuracy in the External Design Specification regarding XOR chain #3 and XOR chain #4. These fixes were added as documentation change #2. Added Documentation Change 3 which documents additional processors supported by the Intel® 3100 Chipset.	June 2007
004	Added Documentation Change 4 which documents an additional Intel® Core™2 Duo processor L7400 supported by the Intel® 3100 Chipset.	June 2007
005	Added Documentation Change 5 which documents an additional Intel® Core™2 Duo processor U7500 supported by the Intel® 3100 Chipset. Added Specification Change 1 to correct the TAP pin VIL maximum level from 0.5 V to 0.35 V.	August 2007
006	For Erratum 24, the workaround was clarified to point customers to the ICH6 BIOS Specification Update, instead of the BIOS Specification. Added 16 Specification Clarifications (4 to 19). Added five Documentation Changes (6 to 10).	November 2007



Preface

This document is an update to the specifications contained in the Affected Documents/ Related Documents table below. This document is a compilation of device and document errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in the Nomenclature section are consolidated into this update document and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Document Title	Location/CDI Number
Intel® 3100 Chipset Datasheet	http://developer.intel.com/design/intarch/datashts/313458.htm
Intel® 3100 Chipset External Design Specification Addendum	Contact your Intel sales representative.
Intel® 3100 Chipset External Design Specification	Contact your Intel sales representative.
Intel® Core™ Duo Processors with Intel® 3100 Chipset Customer Reference Board User Guide	Contact your Intel sales representative.
Intel® Core™ Duo Processor U2500 with Intel® 3100 Chipset Platform Design Guide	Contact your Intel sales representative.

Nomenclature

Errata are design defects or errors. These may cause the Intel® 3100 Chipset to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

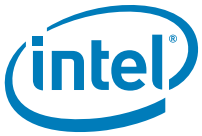
Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Note: Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are

removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).



Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the Intel® 3100 Chipset product. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Plan Fix:	This erratum may be fixed in a future stepping of the product.
Fixed:	This erratum has been fixed in a previous stepping.
No Fix:	There are no plans to fix this erratum.

Row

	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Summary Table of Changes (Sheet 1 of 2)

No.	Stepping		Page	Status	ERRATA
	A0	A1			
1	X	X	12	No Fix	DMA channel source address checking error
2	X	X	12	No Fix	Data corruption after illegal front side bus configuration write
3	X	X	12	No Fix	Incorrect PCI Express* (PEA) link/lane numbers driven in degraded link
4	X	X	12	No Fix	PCI Express* (PEA) enhanced configurations to non-existent devices cause a system hang
5	X	X	13	No Fix	Spurious errors logged during link training events
6	X	X	13	No Fix	DDR2 write offset issue
7	X	X	13	No Fix	Intel® 3100 Chipset fails to train when non-TS1/TS2 training sequences are received
8	X	X	13	No Fix	Configuration transaction may be ignored in the Intel® 3100 Chipset when Configuration Request Retry Status is enabled in PCI Express* (PEA) to PCI/PCI-X bridges
9	X	X	14	No Fix	PCI Express* (PEA) x4 and x8 links may train down to lower width
10	X	X	14	No Fix	END symbol omitted from the last PM_Request_Ack DLLP while entering L2 state on x1 PCI Express* (PEA) link
11	X	X	15	No Fix	SMBSDA and SMBSCL signals pulled down in S5
12	X	X	15	No Fix	Multiple PCI Express* port PEA protocol errors may result in fatal receiver overflow
13	X	X	15	No Fix	System marginalities may result in spurious link-down error events on power state changes
14	X	X	16	No Fix	SATA COMINIT/COMWAKE Detection
15	X	X	16	No Fix	Noise on PCI Express* (PEB) TX coming out of Electrical Idle
16	X	X	16	No Fix	Intel® 3100 Chipset sending less than the minimum number of Power Management Acknowledgements (PMAKs) to SATA
17	X	X	16	No Fix	Advanced Host Controller Interface (AHCI): Improper length Register Device-to-Host FIS
18	X	X	17	No Fix	Split-Lock cycle to LPC space resulting in FSB timeout and IERR
19	X	X	17	No Fix	Intel® 3100 Chipset SATA signal voltage level
20	X	X	17	No Fix	PCI Express* (PEB) completion timer not halting in L1
21	X	X	17	No Fix	PCI Express* (PEB) Extended Tag capability bit
22	X	X	17	No Fix	Intel® 3100 Chipset does not ignore a PCI Express* Null Packet on port PEB
23	X	X	18	No Fix	PCI Express* port PEB Link layer should drop Data Link Layer Packets (DLLPs) with unknown encoding type
24	X	X	18	No Fix	SATA SRST during link power states
25	X	X	18	No Fix	Unsolicited COMINIT while FIS posting pending will corrupt the FIS posting cycle
26	X	X	18	No Fix	USB output voltage
27	X	X	18	No Fix	Intel® 3100 Chipset AHCI PxCMD.CR bit
28	X	X	19	No Fix	Intel® 3100 Chipset PIO setup FIS error
29	X	X	19	No Fix	Intel® 3100 Chipset PCI Express* port PEB surprise removal
30	X	X	19	No Fix	SATA EB buffer overflow should set ERR.E bit instead of ERR.M bit
31	X	X	19	No Fix	PCI Express* port PEB SKP/InitFCx contention
32	X	X	20	No Fix	PCI Express* port PEB downstream ports flag inbound 4 KByte memory read as malformed TLP
33	X	X	20	No Fix	Full Speed USB ISOC End of Packet
34	X	X	20	No Fix	AHCI Host Bus Adapter (HBA) BSY bit set when recovering from fatal error
35	X		20	Fixed	Intel® 3100 Chipset 2 Gbit refresh violation

Summary Table of Changes (Sheet 2 of 2)

No.	Stepping		Page	Status	ERRATA
	A0	A1			
36	X		21	Fixed	Intel® 3100 Chipset lock-up due to internal downstream EDMA and arbitration error
37	X		21	Fixed	System lock condition with numerous split-lock cycles on PCI Express* Port B in conjunction with Heavy PCI Express* traffic on both Port A and Port B
38	X	X	21	No Fix	PCI Express* Port PEB scrambling
39	X		22	No Fix	Behavior of Serial Port Interrupt Enable Register

Specification Changes

No.	Page	SPECIFICATION CHANGES
1	23	TAP VIL maximum level corrections from 0.5 V to 0.35 V

Specification Clarifications

No.	Page	SPECIFICATION CLARIFICATIONS
1	24	16550 compatible serial ports
2	24	Fatal/non-fatal Status of NSI_FERR and NSI_NERR registers
3	27	D31:F0:ACh documentation error
4	27	TMS signal needs pull-up recommendation
5	27	Intel SpeedStep® technology is enabled by processor
6	27	HCLKIN and PEx_CLK slew rates should correlate to rise/fall times
7	28	THRMTRIP# and FERR# are both CMOS 1.05 V signals
8	28	TEST# pin must be no connect if unused
9	28	HACVREF and HDVREF formula fix for reference voltages
10	29	DIMM routing guidelines need to be consistent
11	29	VCCP decoupling guidelines need to be consistent
12	29	HCLKIN 700 mil trace length clarification
13	30	VCCSENSE/VSSSENSE design recommendation
14	30	Access to TPM components not enabled
15	30	TEST1 pin must be pulled to ground
16	31	DPWR# pull-up clarification
17	31	DPRSTP# pull-up guidelines added
18	31	BSEL illustration removed
19	32	CPURST# routing for XDP clarified

Documentation Changes

No.	Page	DOCUMENTATION CHANGES
1	33	SIRI and STRD registers
2	33	XOR chain tables
3	37	Added processor support
4	37	Added L7400 processor support
5	38	Added U7500 processor support
6	39	USB3/2 ports need to be swapped in User's Manuals
7	39	Miscellaneous CAP and RES typos and clarifications
8	40	INIT3_3V# addition to chipset checklist
9	40	PDF page numbers should match Adobe* Reader*
10	40	VREF tolerance fixed to +/-2%

Identification Information

Component Identification via Programming Interface

The Intel® 3100 Chipset can be identified by the following register contents:

Stepping	Vendor ID[1]	Device ID[2]	Stepping ID[3]
A0	8086h	2670h	00h
A1	8086h	2670h	01h

Notes:

1. The Vendor ID corresponds to bits [15:0] of the Vendor ID Register located at offset 00–01h in the PCI B0: D31: F0 configuration space.
2. The Device ID corresponds to bits [15:0] of the Device ID Register located at offset 02–03h in the PCI B0: D31: F0 configuration space.
3. The Stepping ID corresponds to bits [23:16] of the Manufacturer's ID Register located at offset F8h in the PCI B0: D31: F0 configuration space.

Component Marking Information

The Intel® 3100 Chipset stepping can be identified by the following component markings:

Stepping	Q-Spec/S-Spec	Description
A0	Q176	Pb Free Engineering
A0	SL8YC	Pb Free Production
A1	Q699	Pb Free Engineering
A1	SL9PU	Pb Free Production
A1	Q704	Pb Engineering
A1	SL9PV	Pb Production

Errata

1. DMA channel source address checking error

Problem: In the DMA controller memory mapped registers, bit [6] of the DCRs (Descriptor Control Registers Memory Mapped I/O Address Offset 2Ch-2Fh, 6Ch-6Fh, 0ACh-A7h, 0ECh-EFh) for channels 0-3 should be RO, but it is implemented as RW.

Implication: The DMA controller does not implement error checking for this case if this bit is set to '1.'

Workaround: Do not write a '1' to bit [6] of the DCRx for channels 0-3.

Status: No Fix.

2. Data corruption after illegal front side bus configuration write

Problem: When an illegal FSB configuration write occurs (bits [30:24] of the Configuration Address Register [CONFIG_ADDRESS, I/O address 0CF8h] are non-zero), PCI configuration accesses following this write may be corrupted.

Implication: This is a mishandled error case and causes corruption of transactions after this transaction. This is an illegal case.

Workaround: Do not write non-zero values to the PCI configuration address register reserved fields.

Status: No Fix.

3. Incorrect PCI Express* (PEA) link/lane numbers driven in degraded link

Problem: If a failure of receiver detect or bit/symbol lock occurs on lane 0 (lane 7 in the case of a physical lane reversal) while other lanes successfully achieve bit/symbol lock in the early stages of Polling.Active, the Intel® 3100 Chipset will exhibit anomalous lane numbering during the ensuing failed training sequence. Note that this anomalous behavior only occurs in situations where the combination of successful and failing lanes will result in a training failure, and a return to the Polling state.

Implication: When such a failed training is in progress, non-compliant non-PAD lane numbers may be observed on the Intel® 3100 Chipset downstream lanes. The observed behavior may be seen as the Intel® 3100 Chipset attempting a link split.

Workaround: None

Status: No Fix.

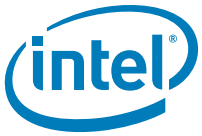
4. PCI Express* (PEA) enhanced configurations to non-existent devices cause a system hang

Problem: A system hang may occur when writing or reading to offsets above 0FFh using the PCI Express* (PEA) enhanced configuration space of a non-existent device.

Implication: An invalid access error will be flagged, and a system hang may result.

Workaround: Polling or testing for devices must be done using offsets below 0FFh. Access must not be issued to offsets above 0FFh unless the targeted device is confirmed present.

Status: No Fix.



5. Spurious errors logged during link training events

Problem: The Intel® 3100 Chipset reports spurious receiver errors during initial link training, after a retrain, or after a secondary bus reset has occurred.

Implication: Spurious receiver errors will be logged in the associated port. There are no negative side affects besides the misreported error.

Workaround: Upon initial training and after each retrain or secondary bus reset, clear the correctable error detected bit of the PCI Express (PEA) Device Status Register (PEADEVSTS, Device 2-3, Function 0, Offset 6E-6Fh bit [0], 1b) and the receiver error status bit of the PCI Express Correctable Error Status Register (CORERRSTS, Device 2-3, Function 0, Offset 110-113h bit [0], 1b). Also clear the PEAFERR/PEANERR bits that flag correctable errors (EXP_FERR/EXP_NERR, Device 2-3, Function 0, Offset 160-163h / 164-167h bit 6, 1b).

Status: No Fix.

6. DDR2 write offset issue

Problem: DQ/DQS signals terminate to a level about 300 mV below VDDQ/2 between write bursts. No functional failures have been observed as a function of this issue.

Implication: Signal integrity issues may be observed.

Workaround: None

Status: No Fix.

7. Intel® 3100 Chipset fails to train when non-TS1/TS2 training sequences are received

Problem: During the PCI Express (PEA) training sequence, if a broken endpoint or a good endpoint on a broken board has correct receiver termination on any lane and transmits signals on that lane that can be seen at the Intel® 3100 Chipset and are not valid TS1/TS2 training sequences, the Intel® 3100 Chipset will fail to train that link.

Implication: The PCI Express specification intends that, if some lanes are transmitting bogus data instead of valid training sequences, those lanes should be treated as broken, and the link should fail down to an acceptable width (such as x1). If lane 0 were failing in this manner, the link would fail to train per the PCI Express specification. If a higher-numbered lane were failing in this manner, the PCI Express specification requires the link attempt to train as a x1 on lane 0—the Intel® 3100 Chipset will not train in this scenario.

Failures are anticipated to occur because of a broken transmitter/receiver path, or a silent transmitter. None of those failure modes will cause the Intel® 3100 Chipset to fail to train, since either the receiver termination will be missing, or the transmitted signals will not be seen at the Intel® 3100 Chipset. In order to see invalid transmitted signals at the Intel® 3100 Chipset, either a logic bug in the other PCI Express endpoint would be required, or a signal integrity issue so severe as to make operation impossible.

Workaround: None

Status: No Fix.

8. Configuration transaction may be ignored in the Intel® 3100 Chipset when Configuration Request Retry Status is enabled in PCI Express* (PEA) to PCI/PCI-X bridges

Problem: Under certain circumstances that include a mix of PCI Express traffic in the presence of completions with Configuration Retry Status (configuration space traffic receiving CRS, and other traffic that is posted / governed by Posted Flow Control credits) on a given PCI Express port, the Intel® 3100 Chipset may ignore and fail to issue an outbound configuration space access indefinitely. This behavior has been observed in configurations with PCI Express to PCI/PCI-X bridge devices under circumstances

where at least one device behind the bridge is active and operational, while at least one other device behind the bridge remains unresponsive to configuration requests for an extended period of time. Such failures ultimately manifest themselves as CPU IERR# assertions, which commonly precipitate a platform reboot. Completions with Configuration Request Retry Status are generally sent by a PCI Express to PCI/PCI-X bridge when it relays configuration space traffic to a PCI/PCI-X device which exhibits a long latency in responding to configuration space traffic. The CRS completion status mechanism is intended to prevent a PCI Express completion timeout from occurring in cases where historical PCI/PCI-X implementations would experience an extended latency without response, but would not generate any timeout or associated error.

Implication: A system hang may occur.

Workaround: To avoid configuration transactions from being ignored, Intel strongly recommends that BIOS should disable Configuration Request Retries in all PCI Express bridge devices. For the Intel® 6700PXH 64-bit PCI Hub, this is accomplished by clearing the Bridge Configuration Retry Enable bit in the Device Control Register (D0:F0,2:R04Ch bit [15]). This bit is cleared by default. Some PCI or PCI-X devices may require a lengthy self-initialization sequence (up to 1.5 sec. as defined by PCI Express Base Specification 1.0a) to complete before they are able to service Configuration Requests after reset. In order to ensure the ability of the system to successfully enumerate PCI devices, BIOS should disable PCI Express Completion Timeout in the root port configuration of the Intel® 3100 Chipset links connected to the Intel® 6700PXH 64-bit PCI Hub, Intel® IOP332 I/O processor, and Intel® 41210 Serial to Parallel PCI Bridge (including add-in cards) by setting the Completion Timeout Timer Disable bit in the Vendor Specific Command Register (D2-7:F0:R045h bit [3]). BIOS should ensure that the Completion Timeout Timer remains enabled (default) for other active PCI Express links. BIOS should also ensure that the Completion Timeout Error Mask is set in the Intel® 3100 Chipset root ports associated with inactive PCI Express links (unpopulated slots or disabled devices).

Status: No Fix.

9. PCI Express* (PEA) x4 and x8 links may train down to lower width

Problem: It has been observed that x4 and x8 links may fail to train to their full link widths. This behavior occurs infrequently. The issue is caused by the Intel® 3100 Chipset exiting the Polling.Active state and entering the Polling.Config state prior to the downstream device entering the Polling.Active state.

Implication: PCI Express ports may fail to train at full width.

Workaround: Intel recommends an algorithm that will issue a Secondary Bus Reset upon a link training failure for 2 ms. The algorithm should support at least three iterations of Secondary Bus Resets.

Status: No Fix.

10. END symbol omitted from the last PM_Request_Ack DLLP while entering L2 state on x1 PCI Express* (PEA) link

Problem: When a PEA x1 link transitions into the L2 state, the Intel® 3100 Chipset may fail to transmit the END symbol of the last PM_Request_Ack DLLP.

Implication: If a downstream device expects an END symbol in the last PM_Request_Ack DLLP from the Intel® 3100 Chipset, it may incorrectly decode the electrical ordered set that follows. Endpoints should expect the COM symbol in the electrical ordered set to indicate a final confirmation to transition the link to the L2 state.

Workaround: None

Status: No Fix.

11. SMBSDA and SMBSCL signals pulled down in S5

Problem: According to SMBus Specification 2.0, the SMBSDA and SMBSCL signals are to float while in the S5 state. Due to device protection circuitry, these signals are pulled down while in the S5 state.

Implication: Devices on auxiliary power such as a BMC that share an SMBus connection with the Intel® 3100 Chipset will not be able to signal on the SMBus in the S5 state due to the signals being pulled down.

Workaround: A mux can be incorporated into the SMBus to disconnect the Intel® 3100 Chipset when the platform goes into the S5 state.

Status: No Fix.

12. Multiple PCI Express* port PEA protocol errors may result in fatal receiver overflow

Problem: If a PCI Express device connected to the Intel® 3100 Chipset port PEA generates multiple transaction layer protocol errors, including unexpected completion packets or malformed Transaction Layer Packets (TLPs) that otherwise pass all link-layer error checking, and have the correct alignment on the interface, the Intel® 3100 Chipset may experience a fatal receiver overflow.

Implication: If the above conditions are met, the Intel® 3100 Chipset may detect and log a fatal receiver overflow error. The Intel® 3100 Chipset behavior in the presence of this error is consistent with the specification, in that continued operation on the port after such an error may be unreliable.

Workaround: Intel recommends avoiding the use of PCI Express devices that generate unexpected completion or malformed TLP protocol violations. If this is unavoidable, the receiver overflow error detected by the Intel® 3100 Chipset may be escalated to a system event (e.g., SERR#) that prevents continued operation on the compromised link.

Status: No Fix.

13. System marginalities may result in spurious link-down error events on power state changes

Problem: On system power state changes (S3 and S5), PCI Express devices are placed in the D3 device power state by the operating system, which results in automatic negotiation with the Intel® 3100 Chipset to enter the L1 link state. In systems where the cumulative noise present at the Intel® 3100 Chipset receiver pins exceeds the Intel® 3100 Chipset receiver threshold for detecting Electrical Idle, the transition into L1 may fail to complete normally; ultimately, resulting in a spurious link-down error from the Intel® 3100 Chipset. If a link-down error (D2-3:F0:O140h, bit [11]) is escalated using a fatal system error (SERR#) mechanism, a blue-screen may result on exposed systems.

The PCI Express specification for Electrical Idle at the receiver is 65 mV peak-peak differential, and characterization of the Intel® 3100 Chipset indicates that some lanes on some devices are marginal with respect to this specification. While L1 failures should be exceedingly rare, Intel recognizes that this specification is difficult to meet and acknowledges the exposure.

Implication: Systems with sufficient noise at the Intel® 3100 Chipset receivers and a BIOS profile that escalates the link-down error as a fatal system event may be exposed to a blue-screen occurrence on system power state transitions. Exposure to the error increases with the cumulative noise (platform noise + silicon noise) present at the Intel® 3100 Chipset receivers when the link is in Electrical Idle. Systems utilizing a BIOS configuration that does not escalate the link-down error as a fatal error are not exposed.

Custom operating systems or future operating systems that independently manage the power state of PCI Express devices outside the scope of system power state transitions would be similarly exposed to link-down errors via the same mechanism. In cases where the destination power state on the attached device is between D0 and D3, any such link-down event constitutes a real error from which software may only recover by fully reconfiguring the devices below the affected link.

Workaround: None

Status: No Fix.

14. SATA COMINIT/COMWAKE Detection

Problem: During Out-Of-Band (OOB) sequencing, the Intel® 3100 Chipset may detect COMINIT/COMWAKE when only two or three bursts of ALIGNs are received from the SATA device instead of the required four bursts as per the SATA Specification 1.0a.

Implication: No known implications—the Intel® 3100 Chipset appropriately handles subsequent ALIGNs.

Workaround: None

Status: No Fix.

15. Noise on PCI Express* (PEB) TX coming out of Electrical Idle

Problem: The PCI Express (PEB) Common Mode Voltage is not stable immediately after Receiver Detect Sequencing when entering Polling.Active from Detect.Active states.

Implication: Common Mode Voltage noise may result in bet errors early in the Polling.Active state. It may result in additional training time before transitioning on to Polling.Configuration.

Workaround: None

Status: No Fix.

16. Intel® 3100 Chipset sending less than the minimum number of Power Management Acknowledgements (PMAKs) to SATA

Problem: The SATA specification requires the Intel® 3100 Chipset to send at least four PMAKs to the SATA device. The Intel® 3100 Chipset sends only three PMAKs before entering a lower power state after the device requests a partial or slumber state on the SATA bus.

Implication: This errata violates the SATA specification but is not expected to cause any functional failures.

Workaround: None

Status: No Fix.

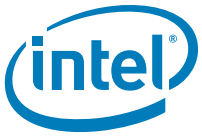
17. Advanced Host Controller Interface (AHCI): Improper length Register Device-to-Host FIS

Problem: If a SATA device sends less than a five dword Register Device-to-Host FIS, the Intel® 3100 Chipset will correctly respond with RERR but may not be able to accept any further FISes from the device.

Implication: The SATA bus will hang. This only applies while operating in AHCI mode. No known devices use Register Device-to-Host FIS sizes less than five dwords, as these are not allowed by the SATA Specification 1.0a.

Workaround: The AHCI driver should reset the bus by sending COMRESET per the AHCI specification.

Status: No Fix.



18. Split-Lock cycle to LPC space resulting in FSB timeout and IERR

Problem: The Intel® 3100 Chipset may not properly handle split locked cycles to the LPC when a PHOLD sequence is going on concurrently. The hang occurs when the second split lock memory read request is sent out on the NSI but never receives a completion.

Implication: The system could hang. This issue has only been replicated using a synthetic test environment and has not been reported using commercially available hardware/ software.

Workaround: None

Status: No Fix.

19. Intel® 3100 Chipset SATA signal voltage level

Problem: The Intel® 3100 Chipset SATA transmit buffers have been designed to maximize performance and robustness over a variety of routing scenarios. As a result, the Intel® 3100 Chipset SATA transmit signalling voltage levels may exceed the maximum motherboard TX connector and device RX connector voltage specification (section 6.6.2 of the SATA Specification 1.0a).

Implication: No known implications.

Workaround: None

Status: No Fix.

20. PCI Express* (PEB) completion timer not halting in L1

Problem: The Intel® 3100 Chipset PCI Express completion timer does not halt when the link enters the L1 state. This affects the port PEB.

Implication: The Intel® 3100 Chipset will flag a completion timer error.

Note: This requires a device that is not fully compliant with the PCI Express specification and has only been replicated in a synthetic test environment.

Workaround: None

Status: No Fix.

21. PCI Express* (PEB) Extended Tag capability bit

Problem: The Intel® 3100 Chipset incorrectly has the PCI Express Extended Tags Supported capability bit (D28:F0/1/2/3:Offset 44h:bit [5]) set to '1,' though the Intel® 3100 Chipset does not support Extended Tags.

Implication: Software will not be able to implement Extended Tags support.

Workaround: None

Status: No Fix.

22. Intel® 3100 Chipset does not ignore a PCI Express* Null Packet on port PEB

Problem: If the Intel® 3100 Chipset receives a PCI Express Null packet, it should drop the packet and not perform sequence number checking or respond with any ACK or NAK DLLP. The Intel® 3100 Chipset still performs sequence number checks for Null packets and may respond with an ACK or NAK depending on the result of the check.

Implication: The Intel® 3100 Chipset port PEB may send an ACK or NAK DLLP in response to a Null packet. This may degrade link performance due to unnecessary retries.

Workaround: None

Status: No Fix.

23. PCI Express* port PEB Link layer should drop Data Link Layer Packets (DLLPs) with unknown encoding type

Problem: A received DLLP which is not corrupt, but which uses unsupported DLLP Type encoding is discarded without further action. This is not considered an error.

Implication: If the Intel® 3100 Chipset interprets this as an NAK, a needless replay may occur. This bug violates the PCI Express specification but is not expected to cause any functional failures.

Workaround: None

Status: No Fix.

24. SATA SRST during link power states

Problem: When exiting SATA link partial or slumber states, the Intel® 3100 Chipset may not send a SRST when instructed by software.

Implication: The device will not appear to software until SRST is retried.

Workaround: Refer to the latest ICH6 BIOS Specification Update for workaround details.

Status: No Fix.

25. Unsolicited COMINIT while FIS posting pending will corrupt the FIS posting cycle

Problem: Only in AHCI mode, the SATA controller may post a FIS incorrectly if either an unsolicited COMINIT arrives or if software performs a post reset, while FIS posting is pending internally.

Note: This has only been replicated in a synthetic test environment and has not been reproduced in a production environment.

Implication: A malformed TLP is delivered and inappropriate data is delivered on the next upstream cycle.

Workaround: None. The system can be configured to detect this anomalous condition and reset the system to prevent this data migration. Refer to the latest BIOS Specification for workaround details.

Status: No Fix.

26. USB output voltage

Problem: The Intel® 3100 Chipset High Speed USB 2.0 V_{HSOL} and V_{HSOH} may not meet the USB 2.0 specification. The expected V_{HSOL} is 60 mV and the maximum expected V_{HSOH} is 470 mV.

Implication: No known implications.

Workaround: None

Status: No Fix.

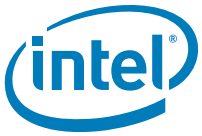
27. Intel® 3100 Chipset AHCI PxCMD.CR bit

Problem: If a Task File fatal error occurs during a SATA.AHCI transfer, the Intel® 3100 Chipset will not automatically clear the PxCMD.CR bit, as required by the AHCI Specification 1.0, until the AHCI driver software follows the specification-defined recovery mechanism.

Implication: No known implications as AHCI compliant driver software will cause the Intel® 3100 Chipset to clear the CR bit during error recovery

Workaround: None

Status: No Fix.



28. Intel® 3100 Chipset PIO setup FIS error

Problem: The Intel® 3100 Chipset SATA AHCI controller may set the ERR.T and PxIS.IFS bits when a link error (such as a CRC error) or the Intel® 3100 Chipset SATA receiver error occurs on a PIO Setup FIS, instead of setting the PxIS.INFS bit, as defined by the AHCI Specification 1.0.

Implication: A spurious interrupt is generated, and the AHCI driver software will detect the error and retry.

Workaround: None

Status: No Fix.

29. Intel® 3100 Chipset PCI Express* port PEB surprise removal

Problem: After eight surprise removal or non-software initiated link-down events on a PCI Express port PEB without a platform reset, the Intel® 3100 Chipset may not be able to receive completions from the device on the PCI Express link.

Implication: The system may hang.

Note: Issue requires multiple PCI Express drives to be populated in the system with simultaneous upstream requests. Software must also de-program the PCI Express port PEB number that experienced the event before hardware is able to fully respond to the link-down condition. Known software does not de-program the surprise removal port before hardware responds. This issue has only been observed in a simulation environment.

Workaround: Perform a platform reset.

Status: No Fix.

30. SATA EB buffer overflow should set ERR.E bit instead of ERR.M bit

Problem: The Intel® 3100 Chipset erroneously sets the PxSERR:[M] (Recovered Communications Error) when the internal elasticity buffer experiences an overflow or if a miss-align is detected after PhyRDY is detected. A miss-align may happen during resume from the Partial or Slumber link PM states and will cause the M-bit to be erroneously set.

Implication: As a result of M-bit setting while resuming, the host will set the Interface Non-Fatal Status (INFS) bit since it happens while the interface has no Frame Information Structure being transferred or received. INFS is expected to be recoverable by S/W (mostly ignored) and should not have an impact to subsequent command execution. No restart of the controller is needed in this case.

Workaround: None needed.

Status: No Fix.

31. PCI Express* port PEB SKP/InitFCx contention

Problem: During PCI Express port PEB initialization, if a SKP is being transmitted immediately before a InitFCx DLLP, then a partial InitFCx may be transmitted.

Implication: A slight delay (less than 100 ns) may occur during link initialization. The device may report correctable errors. InitFCx will automatically be repeated.

Workaround: None

Status: No Fix.

32. PCI Express* port PEB downstream ports flag inbound 4 KByte memory read as malformed TLP

Problem: PCI Express downstream ports (PEB1 and PEB2) flag inbound 4 kByte memory read requests as malformed TLPs. The downstream ports will log the malformed TLP error and discard the memory read requests. This condition could occur if downstream devices can generate read request up to 4 KByte.

Implication: Inbound 4 KByte memory read request will fail, and the downstream device will lose flow control credit.

Workaround: Refer to the latest BIOS Specification for workaround details.

Status: No Fix.

33. Full Speed USB ISOC End of Packet

Problem: If a Full-speed USB ISOC OUT transaction occurs very late in the USB frame such that the payload cannot be contained in the frame, then a bit stuff error is created as defined in the USB 2.0 specification and flagged to both host software and device. When this occurs, and a specific data pattern is present, then the End of Packet (EOP) will not be sent. In this event, devices attached to that UHCI controller may not detect the subsequent Start of Frame (SOF) due to lack of EOP.

Implication: None. The resulting bit stuff error and device not detecting SOF are recoverable events by USB 2.0 system design.

Note: USB ISOC traffic and SOF packets are not inaccessibly data coherent by definition of the protocol. This issue has only been replicated in a synthetic test environment and has not been reproduced in known system configurations.

Workaround: None.

Status: No Fix.

34. AHCI Host Bus Adapter (HBA) BSY bit set when recovering from fatal error

Problem: During an AHCI fatal error condition, if the device signals a Task File Error (TFES), the Intel® 3100 Chipset may not be able to recover correctly after software performs the AHCI specification-defined fatal error recovery mechanism.

Implication: The SATA port will appear busy resulting in the device being inaccessible.

Workaround: The AHCI driver should toggle the ST bit to '1' and back to '0' upon detecting TFES bit set after the ST bit is cleared.

Status: No Fix.

35. Intel® 3100 Chipset 2 Gbit refresh violation

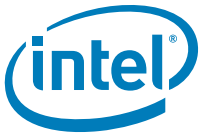
Problem: The Intel® 3100 Chipset violates the auto refresh cycle time (T_{rfc}) specification for 2 Gbit DDR2 400 memory devices. The Intel® 3100 Chipset currently has a refresh cycle time of 27 clocks (135 ns); however, a minimum of 39 clocks (195 ns) is necessary for 2 Gbit devices.

Implication: The Intel® 3100 Chipset will not support 2 Gbit memory devices.

Note: This has only been replicated in a synthetic test environment and has not been reproduced in a production environment since reliable 2 Gbit based DIMM samples are not yet available.

Workaround: None.

Status: Fixed in A1 stepping. For the steppings affected, see the "Summary Table of Changes" table.



36. Intel® 3100 Chipset lock-up due to internal downstream EDMA and arbitration error

Problem: The Intel® 3100 Chipset will lock-up due to simultaneous downstream transactions destined to the same PCI Express port PEA link. The simultaneous downstream transactions that must occur are a FSB or Memory Read Request (MRR), an EDMA memory to PCI Express port A request, and a PCI Express port A peer-to-peer transaction. The PCI Express port A must be configured as a 2x4 or 2x1 port for this event to occur.

Implication: The FSB or MRR transaction has the highest priority and will be serviced first by the Arbiter. At the same time the Arbiter believes the EDMA request has also been serviced. Because the EDMA request was not serviced its request is still pending. The Arbiter is unaware of the pending EDMA request and the Intel® 3100 Chipset will not allow anymore requests through the system until the pending EDMA request is serviced, at this point the system hangs.

Workaround: Two workarounds are available for this erratum.

- Configure the PCI Express Port PEA as 1x8, 1x4, or 1x1.
- Disable EDMA memory to I/O transactions completely.

Status: Fixed in A1 stepping. For the steppings affected, see the "Summary Table of Changes" table.

37. System lock condition with numerous split-lock cycles on PCI Express* Port B in conjunction with Heavy PCI Express* traffic on both Port A and Port B

Problem: A hang condition occurs when the processor issues split-locked request (R-R-W-W) to any PCI express device on Port B combined with heavy traffic on both Port A and Port B. This issue can be noted under the following scenario:

- Downstream split-lock cycle destined to a device on Port B
- Port A sending upstream snoop and non-snoop transactions during the lock on Port B
- Port B sends upstream non-snoop requests during the lock on Port B

Implication: A hang condition occurs

Workaround: Refer to the latest BIOS Specification for workaround details. Upstream ports on PEA will always snoop the FSB with this workaround.

Status: Fixed in A1 stepping: For the steppings affected, see the "Summary Table of Changes" table.

38. PCI Express* Port PEB scrambling

Problem: While entering the recovery state, the port PEB stops scrambling two symbols before the first Training Sequence (TS).

Implication: When these non-scrambled symbols are received by the endpoint, the de-scrambler of the endpoint will observe two symbols of random data. The first symbol of TS1 will reset the endpoint's de-scrambler so that the endpoint should recognize the TS1 and TS2 ordered-sets being transmitted and move into the Recovery state as planned.

Note: There is no system level impact if the endpoint is PCI Express Specification 1.0a compliant in ignoring the random data.

Workaround: None

Status: No Fix.

39. Behavior of Serial Port Interrupt Enable Register

Problem: The Serial Port Interrupt Enable Register (IER) bit 1 (Transmit Data request Interrupt Enable) will not change status if the bit has been set previously.

Implication: Will not cause an interrupt if the register bit has been set already.

Workaround: Customers may be able to implement a BIOS workaround to clear out the bit IER bit 1 to '0' before programing the bit to '1'.

Status: No fix.

Specification Changes

1. TAP VIL maximum level corrections from 0.5 V to 0.35 V

Issue: The VIL maximum level for the TAP pins on the LE/BF3100MICH was incorrectly identified as 0.5 V. The correct VIL maximum level is 0.35 V. This change affects the TAP pins (signal groups 63, 65, 66) TRST#, TMS, TDI, TCK, TEST#, DEBUG[7:0]. These pins are typically used during product evaluation and/or production test. Intel does not anticipate any impact to customer applications. A Production Change Notification (PCN 107781-00) was published on 8/7/07 to notify customers that the correct VIL level is 0.35 V and that this change goes into effect against all material shipped after 9/7/07.

Affected Docs: Intel® 3100 Chipset Datasheet and Intel® 3100 Chipset External Design Specification Addendum are both updated with the same changes as follows:

1. Table 1105 (TAP DC Characteristics) in Section 32.4 of Intel® 3100 Chipset Datasheet is updated per changes to Vil Max in the following table.
2. Table 27 (TAP DC Characteristics) in Section 5.0 of the Intel® 3100 Chipset External Design Specification Addendum is updated per changes to Vil Max in the following table.

Sig Group	Symbol	Parameter	Min	Max	Units	Notes
(63)	Vil	Input low voltage		Change from 0.5 to 0.35	V	
(65), (66)	Vil	Input low voltage	-0.3	Change from 0.5 to 0.35	V	

Specification Clarifications

1. 16550 compatible serial ports

Section 1.8.15 - Serial Port and Section 31.2 - Features in the *Intel*® 3100 Chipset *Datasheet* makes references to "Two full function 16550 compatible serial ports". The serial ports of Intel® 3100 Chipset are not 100 percent compatible with other 16550 standard devices. Some examples of this are seen as follows:

• Section 31.6.4.3, Interrupt Enable Register (IER)

— "Note: The use of bit 4 and 5 is different from the register definition of standard 16550."

• Section 31.6.4.5, FIFO Control Register (FCR)

—"Note: The use of bit 6 and 7 is different from the register definition of standard 16550."

If any system or software designer assumes that they are compatible with other 16550 standard devices and does not follow the specifications for the Serial I/O Unit in the *Intel*® 3100 Chipset *Datasheet*, errors or undesired behaviors may be observed.

2. Fatal/non-fatal Status of NSI_FERR and NSI_NERR registers

The NSI First Error (NSI_FERR) Registers in sections 143.2.1.13 does not mention the fatal/non-fatal status of its bits. Table 85226 will be replaced as follows. The same would apply for the NSI Next Error (NSI_NERR) Register.

Note: If two errors occur within 1 clock cycle of each other in the NSI, the first error will get logged into FERR but the error on the next clock edge may or may not get logged into the NERR. All follow on errors after the second cycle will get captured into the NERR

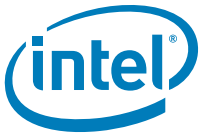


Table 1. Offset 48 - 4Bh: NSI_FERR - NSI First Error Register (Sheet 1 of 3)

Device: 0 ***Function:*** 1

Offset: *48 - 4Bh* ***Size:*** *32 bit*

Default Value: *0000_0000h*

Bits	Name	Description	Reset Value	Access
31:30	Reserved	Reserved	00b	
29	UR	**Unsupported Request [STICKY]:** This bit is sticky through reset. 0 = Cleared by writing a '1' to the bit location. 1 = Unsupported Request detected.(NON-FATAL.)	0b	RWC
28	Reserved	Reserved	0b	
27	MTLP	**Malformed TLP Status [STICKY]:** Malformed TLP errors include: data payload length issues, byte enable rule violations, and various other illegal field settings. This bit is sticky through reset. 0 = Cleared by writing a '1' to the bit location. 1 = Malformed TLP detected.(FATAL.)	0b	RWC
26	ROVF	**Receiver Overflow Status [STICKY]:** checks for overflows on the following upstream queues: posted, non-posted, and completion. This bit is sticky through reset. 0 = Cleared by writing a '1' to the bit location. 1 = Receiver Overflow detected.(FATAL)	0b	RWC
25	UEC	**Unexpected Completion Status [STICKY]:** This bit is set when the device receives a completion which does not correspond to any of the outstanding requests issued by that device. This bit is sticky through reset. 0 = Cleared by writing a '1' to the bit location. 1 = Unexpected Completion detected.(NON-FATAL)	0b	RWC
24	CA	**Completer Abort Status [STICKY]:** If a request received violates the specific programming model of this device, but is otherwise legal, this bit is set. This bit is sticky through reset. 0 = Cleared by writing a '1' to the bit location. 1 = Completer Abort detected.(NON-FATAL)	0b	RWC
23	CT	**Completion Timeout Status [STICKY]:** The Completion Timeout timer must expire if a Request is not completed in 50 ms, but must not expire earlier than 50 µs. When the timer expires, this bit is set. This bit is sticky through reset. 0 = Cleared by writing a '1' to the bit location. 1 = Completion timeout detected.(NON-FATAL)	0b	RWC
22	Reserved	Reserved	0b	
21	PTLP	**Poisoned TLP Status [STICKY]:** This bit when set indicates that some portion of the TLP data payload was corrupt. This bit is sticky through reset. 0 = Cleared by writing a '1' to the bit location. 1 = Poisoned TLP detected.(NON-FATAL)	0b	RWC
20	Reserved	Reserved	0b	
19	DLPE	**Data Link Protocol Error Status [STICKY]:** This bit is set when an ACK/NAK received does not specify the sequence number of an unacknowledged TLP, or of the most recently acknowledged TLP. This bit is sticky through reset. 0 = Cleared by writing a '1' to the bit location. 1 = Data Link Protocol Error detected.(FATAL)	0b	RWC
18:16	Reserved	Reserved	0b	

Table 1. Offset 48 - 4Bh: NSI_FERR - NSI First Error Register (Sheet 2 of 3)

Device: 0 ***Function:*** 1

Offset: *48 - 4Bh* ***Size:*** *32 bit*

Default Value: *0000_0000h*

Bits	Name	Description	Reset Value	Access
15	RTTO	**Replay Timer Timeout Status [STICKY]:** The replay timer counts time since the last ACK or NAK DLLP was received. When the timer expires, this bit is set. This bit is sticky through system reset. 0 = Cleared by writing a '1' to the bit location. 1 = Replay Timer timeout detected.(NON-FATAL)	0b	RWC
14	Reserved	Reserved	0b	
13	RNRO	**REPLAY_NUM Rollover Status [STICKY]:** A 2-bit counter counts the number of times the retry buffer has been retransmitted. When this counter rolls over, this bit is set. This bit is sticky through system reset. 0 = Cleared by writing a '1' to the bit location. 1 = REPLAY_NUM rollover detected.(NON-FATAL)	0b	RWC
12	BDLLP	**Bad DLLP Status [STICKY]:** This bit is set when the calculated DLLP CRC is not equal to the received value. Also included are 8b/10b errors within the TLP including wrong disparity. An invalid sequence number also sets this bit. This bit is sticky through system reset. 0 = Cleared by writing a '1' to the bit location. 1 = Bad DLLP detected.(NON-FATAL)	0b	RWC
11	BTLP	**Bad TLP Status [STICKY]:** 0 = The calculated TLP CRC is equal to the received value. 1 = The calculated TLP CRC is not equal to the received value. Also included are 8b/10b errors within the TLP including wrong disparity, and invalid sequence numbers.(NON-FATAL)	0b	RWC
10	Reserved	Reserved	0b	
09	RCVRE	**Receiver Error Status [STICKY]:**Data is delivered over PCI Express via packets built out of 8b/10b symbols. This error is set for problems with the packet framing around these symbols or with symbols received outside of recognized packets. This bit is sticky through system reset. 0 = Cleared by writing a '1' to the bit location. 1 = Receiver Error detected.(NON-FATAL)	0b	RWC
08	Reserved	Reserved	0b	
07	FEMR	**Fatal Error Message Received:** 0 = No Fatal Error Message Received over the NSI link. 1 = Fatal Error Message Received over the NSI link.(FATAL)	0b	RWC
06	NEMR	**Non-Fatal Error Message Received:** Non-Fatal Error Message Received over the NSI link. 0 = No Non-Fatal Error Message Received over the NSI link. 1 = Non-Fatal Error Message Received over the NSI link.(NON-FATAL)	0b	RWC
05	CEMR	**Correctable Error Message Received:** Correctable Error Message Received over the NSI link. 0 = No Correctable Error Message Received over the NSI link. 1 = Correctable Error Message Received over the NSI link.(NON-FATAL)	0b	RWC
04:03	Reserved	Reserved	00b	

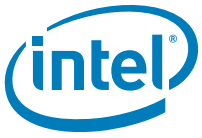


Table 1. Offset 48 - 4Bh: NSI_FERR - NSI First Error Register (Sheet 3 of 3)

Device: 0 ***Function:*** 1
Offset: *48 - 4Bh* ***Size:*** *32 bit*
Default Value: *0000_0000h*

Bits	Name	Description	Reset Value	Access
02	PED	**Parity Error Detected during parity conversion from CTB:** Parity Error detected on data received from the core. 0 = No Parity Error detected on data received from the core. 1 = Parity Error detected on data received from the core.(NON-FATAL)	0b	RWC
01	Reserved	Reserved	0b	
00	LD	**Link Down:** 0 = Link has not transitioned from DL_UP to DL_DOWN. 1 = Link transitioned from DL_UP to DL_DOWN.(FATAL)	0b	RWC

3. D31:F0:ACh documentation error

Register D31:F0:ACh as mentioned in the Base Address bits 15:4 of the LPC Generic Decode Range 2 Register (LG2) is not supported.

4. TMS signal needs pull-up recommendation

Issue: There is an error in Section 3.3.3 of Debug Port Design titled “TMS Routing Guidelines” which requires the following change:

FROM:

- This signal must be pulled-down with a 51 ohm 5% resistor.

TO:

- This signal must be pulled-up to 1.05 V with a 51 ohm 5% resistor.

Affected Docs: Debug Port Design Guide for Intel® 3100 Chipset Systems (Nov. 2006)

5. Intel SpeedStep® technology is enabled by processor

Issue: The reference to Intel SpeedStep® technology needs to be clarified as follows:

FROM:

- Enhanced Intel SpeedStep® Technology is not supported.

TO:

- Enhanced Intel SpeedStep® Technology is a processor-enabled technology, and it does not involve the Intel® 3100 Chipset.

Affected Docs: Section 21.2.7 in the Intel® 3100 Chipset External Design Specification (Jan. 2007) and Section 20.2.7 in the Intel® 3100 Chipset Datasheet (Jun. 2007)

6. HCLKIN and PEx_CLK slew rates should correlate to rise/fall times

Issue: The published slew rates for both HCLKIN and PEx_CLK in Tables 46 and 47 should correlate to calculated slew rates derived from the rise/fall times specified in these same tables. The note under these tables states “Rise and fall times, and slew rates, are measured single ended between 245 mV and 455 mV of the clock swing.” This swing equates to 210 mV, resulting in the following calculated slew rates:

- Slew Rate (min) = 210 mV swing / 700 ps max = 0.3 V/ns
- Slew Rate (max) = 210 mV swing / 175 ps (min) = 1.2 V/ns

All 4 occurrences of slew rates for HCLKIN and PEx_CLK within Tables 46 and 47 need to be changed as follows:

FROM:

- Min=0.5 V/ns, Max=2.0 V/ns

TO:

- Min=0.3 V/ns, Max=1.2 V/ns

Affected Docs: Intel® 3100 Chipset External Design Specification Addendum (Feb. 2007)

7. THRMTRIP# and FERR# are both CMOS 1.05 V signals

Issue: There are several instances were both THRMTRIP# and FERR# are incorrectly referenced as either CMOS3_3 or CMOS1_5 signal types. Both of these signals are CMOS 1.05 V signals and the following clarifications need to be made.

Intel 3100 Chipset Datasheet clarifications:

- Table 1089, change THERMTRIP# Signal Type from CMOS3_3 to CMOS1_05
- Table 1108, change THERMTRIP# Signal Type from CMOS3_3 to CMOS1_05
- Table 1085, change FERR# Signal Type from CMOS1_5 to CMOS1_05
- Table 1107, change FERR# Signal Type from CMOS1_5 to CMOS1_05

Note: The Intel 3100 Chipset EDS Addendum should also include these identical changes.

Affected Docs: Intel® 3100 Chipset Datasheet (Jun. 2007) and Intel® 3100 Chipset External Design Specification Addendum (Feb. 2007)

8. TEST# pin must be no connect if unused

Issue: The TEST# pin in the Schematic Checklist Table needs the following clarification:

FROM:

- TEST# If unused, can be left as no connect

TO:

- TEST# If unused, this pin MUST be left as a no connect.

Affected Docs: Table 93 in the Intel® Pentium® M Processor on 90nm process and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), and Table 94 in the Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), and Table 96 in the Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

9. HACVREF and HDVREF formula fix for reference voltages

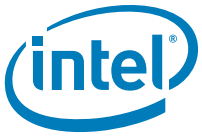
Issue: The formula and 0.63 multiplier for HACVREF and HDVREF min/non/max reference voltages needs to be fixed as follows:

FROM:

- Min 0.98*1.05
- Nom 0.63*VTT
- Max 1.02*1.05

TO:

- Min ..... 0.98*(0.646*VTT)
- Nom ..... (0.646*VTT)



- Max ..... 1.02*(0.646*VTT)

Affected Docs: Table 1100 in the Intel® 3100 Chipset Datasheet (Jun. 2007) and Table 22 in the Intel® 3100 Chipset External Design Specification Addendum (Feb. 2007)

10. DIMM routing guidelines need to be consistent

Issue: The DIMM to DIMM routing guidelines for lengths (B=C=D) in both the Data Signal Group Table and the Address/Command Signal Group Table should specify consistent guidelines of 1.12 - 1.9 inches. In addition, these same two Tables need the B parameter expanded to B=C=D. In summary, two Tables in each published Intel 3100 Chipset Platform Design Guide need the following clarifications:

FROM:

- B = 1.2 - 1.9 inch = Data Signal Group Table
- B = 1.12 - 1.19 inch = Addr/Command Signal Group Table

TO:

- B=C=D = 1.12 - 1.9 inch = Data Signal Group Table
- B=C=D = 1.12 - 1.9 inch = Addr/Command Signal Group Table

Affected Docs: Table 45 and 55 in the Intel® Pentium® M Processor on 90nm process and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), and Table 46 and 56 in the Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), and Table 48 and 58 in the Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

11. VCCP decoupling guidelines need to be consistent

Issue: The VCCP decoupling recommendation per the processor schematic checklist in Table 95 of the Platform Design Guide differs from the VCCP decoupling guidelines per Table 93 of this same Platform Design Guide. Table 95 is in-correct and needs to be changed to the following:

FROM:

Decouple with six 0.1 µF ±20% capacitors and one 220 µF ±10% capacitor.

TO:

Decouple with the following:

- One 150 µF near processor
- Two 150 µF near MCH
- Ten 0.1 µF next to processor
- Three 22 µF near MCH
- Two 0.1 µF under the MCH opposite the die region

Affected Docs: Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

12. HCLKIN 700 mil trace length clarification

Issue: In Table 10, the Parameter titled “Host_CLK Routing Length Matching from Clock Driver to Processors and Clock Driver to the Intel® 3100 Chipset” needs to be changed as follows:

FROM:

Intel® 3100 Chipset HCLKIN pin-to-pin trace length must be 425±10 mils (375 mils for BGA) longer than the processor BCLK pin-to-pin traces.

TO:

Intel® 3100 Chipset HCLKIN pin-to-pin trace length must be 700±10 mils longer than the processor BCLK pin-to-pin traces.

Affected Docs: Intel® Pentium® M Processor on 90nm process and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

13. VCCSENSE/VSSSENSE design recommendation

Issue: The design guides for VCCSENSE/VSSSENSE are dependent on the recommendations of the voltage regulator manufacturers. Therefore, Section 6.9 of the Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide needs to be identical to Section 6.9 of all Intel 3100 Chipset Platform Design Guides, changed to the following:

Section 6.9 Processor VCCSENSE/VSSSENSE Design Recommendation

See an Intel representative for IMVP-VI

Affected Docs: Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

14. Access to TPM components not enabled

Issue: All three Intel 3100 Chipset Development Kit User's Manuals include one TPM overview section that summarizes TPM capabilities on the Development Kit. Although TPM components exist on our platform, access to these TPM components on the LPC (Low Pin Count) bus is not currently enabled by the BIOS. A second paragraph needs to be added to this TPM section to clarify TPM capabilities, as follows:

Trusted Platform Module (TPM)

The Trusted Platform Module (TPM) is a component of the platform that is specifically designed to enhance platform security above and beyond the capabilities of today's software. It provides protected space for key operations and other security critical tasks. Using both hardware and software, the TPM protects encryption and signature keys at their most vulnerable stages of operation, for instance, when the keys are being used in an unencrypted plain text form. The TPM is specifically designed to shield unencrypted keys and platform authentication information from software-based.

Add the following second paragraph.

Although all Development Kits include TPM hardware connected to the Intel 3100 Chipset LPC (Low Pin Count) bus, the platform BIOS does not currently support the enabling of TPM access to hardware located on the LPC. Therefore, all memory access cycles to 0xFED40000-0xFED40FFF (per Table 100 in the Intel 3100 Chipset Datasheet) are driven out on to the PCI to PCI Bridge where they are dropped. Customers need to work with their BIOS vendor to integrate and then enable the TPM feature.

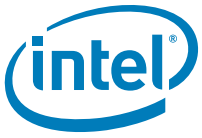
Affected Docs: Intel® Pentium® M Processor on 90nm Process and Intel® 3100 Chipset Development Kit User's Manual (Jan. 2007), Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Development Kit User's Manual (Jan. 2007), Intel® Core™2 Duo Processor and Intel® Core™ Duo Processor and Intel® 3100 Chipset CRB User's Manual (June 2006)

15. TEST1 pin must be pulled to ground

Issue: The Processor Schematic Checklist recommendation for the TEST1 pin needs to be more firm, per following change:

FROM:

- TEST1: Stuffing option with pull-down to Vss through a 1K ohm +/-5% resistor



TO:

- TEST1: MUST pull down to Vss through 1K ohm +/-5% resistor

Affected Docs: Table 93 in the Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), and Table 95 in the Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

16. DPWR# pull-up clarification

Issue: The processor DPWR# signal is not supported by the Intel 3100 Chipset and can be left as either a no connect or can be pulled up to VCCP using a 1K ohm +/- 5% resistor as implemented for test purposes on the Intel 3100 Chipset development kit. Two of the Intel 3100 Chipset Platform Design Guides state that the DPWR# pin MUST be left as a no connect. This firm guideline needs to be more optional for this DPWR# signal, per following changes:

The table titled “Termination for unused processor signals” needs to have following note added for the DPWR# signal:

- DPWR# is not supported by the Chipset and is disabled on the Customer Reference Board by pulling the processor TEST1 pin to VSS with a 1K ohm ±5%.

The “Processor Schematic Checklist” Table for DPWR# also requires the following change:

- FROM: This signal must be left as no connect.
- TO: This signal can be left as no connect.

Affected Docs: Table 40 and 92 in the Intel® Pentium® M Processor on 90nm process and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), and Table 43 and 95 in the Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

17. DPRSTP# pull-up guidelines added

Issue: Guidelines for the DPRSTP# Processor Signal are not published. The Processor Schematic Checklist table needs to have a row added (within the other signals section) identifying the following DPRSTP# design recommendation:

- DPRSTP# Pull-up to VCCP using a 1K 5% resistor

Affected Docs: Table 95 in the Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

18. BSEL illustration removed

Issue: Section 6.11 of the Platform Design Guide includes a Figure 40 titled “Frequency Select Strapping Options” that is mis-leading and will be removed. This figure illustrates BSEL connections that do not represent proper BSEL guidelines as implemented on the Customer Reference Board. The following updates need to be made to Section 6.11.

In Section 6.11, delete Figure 40, keep Tables 40 and 41, and keep the Note.

In Section 6.11, the first paragraph should also be changed to the following:

The BSEL circuit determines the FSB frequency and must be strapped correctly for correct operation as shown per Table 40 and Table 41, using either 1K ohm 5% pull-up or pull-down resistors as summarized per following guidelines:

For 133 MHz FSB Operation:

- CHIPSET CPU_SEL<2> Pull-down to GND using 1K ohm 5% Resistor
- CHIPSET CPU_SEL<1> Pull-down to GND using 1K ohm 5% Resistor
- CHIPSET CPU_SEL<0> Pull-up to VCC1_5 using 1K ohm 5% Resistor

- CK409 FS_A Pull-up to VCC3_3 using 1K ohm 5% Resistor
- CK409 FS_B Tie to GND directly

For 166 MHz FSB Operation:

- CHIPSET CPU_SEL<2> Pull-down to GND using 1K ohm 5% Resistor
- CHIPSET CPU_SEL<1> Pull-up to VCC1_5 using 1K ohm 5% Resistor
- CHIPSET CPU_SEL<0> Pull-up to VCC1_5 using 1K ohm 5% Resistor
- CK409 FS_A Pull-up to VCC3_3 using 1K ohm 5% Resistor
- CK409 FS_B Pull-up to VCC3_3 using 1K ohm 5% Resistor

Affected Docs: Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

19. CPURST# routing for XDP clarified

Issue: Section 6.6.1 titled “Processor RESET# Signal” as published in all three Intel 3100 Chipset Platform Design Guidelines includes a third paragraph related to CPURST# and XDP Routing Guidelines that needs to be clarified to match the illustration of the Figure within the same Section 6.6.1. This entire third paragraph is changed as follows:

FROM:

The CPURST# signal from Intel 3100 Chipset must fork out. Do not route one trace from Intel 3100 Chipset pin and then T-split towards the processor’s RESET# pin as well as towards the Rs resistive termination network placed next to the debug port connector. The debug port operation requires the matching of L2 - L1 length to the length of the processor’s BPM[3:0]# signals length within ±50 ps. Rs must use 5% tolerant resistors. An optional voltage translation logic (Figure 38) can be used for external receivers that are not VCCP (1.05 V) tolerant. All trace spacing must be 1:3. Max breakout of 900 mils with 1:1 spacing.

TO:

The CPURST# signal from Intel 3100 Chipset must be routed to the processor RESET# signal maintaining the length requirements of L1. The CPURST# signal from the processor should then be routed to the Voltage Translation Logic maintaining the length requirements of L2. The CPURST# signal from the Voltage Translation Logic should then be routed to the XDP debug port connector through a 1K ohm +/- 5% Rs series resistor maintaining length guidelines of L3 and L4. The use of a 51.1 ohm +/- 5% Rtt pull-up resistor to VCCP should only be used if the output circuit of the Voltage Translation Logic is open-drain. All routing length requirements for CPURST# are defined within the table included in this section.

Affected Docs: Intel® Pentium® M Processor on 90nm process and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

Documentation Changes

1. SIRI and STRD registers

The following tables will be added in two separate sections proceeding Sections 3029.1.6.2. These registers are necessary to enter SATA test mode.

Table 2. Offset A0h: SIRI – SATA Indexed Register Index

Device: 31 ***Function:*** 2
Offset: A0h ***Size:*** 8 bit
Default Value: *00h* ***Power Well:*** Core

Bits	Name	Description	Reset Value	Access
07:02	IDX	**Index:** 6-bit index pointer into the SATA Indexed Register space. Data is written into and read from the STRD register. This points to a dWord register. The byte enables on the STRD register affect what is written.	00h	RW
01:00	Reserved	Reserved	00	

Table 3. Offset A4 - A7h: STRD – SATA Indexed Register Data

Device: 31 ***Function:*** 2
Offset: A4 - A7h ***Size:*** 32 bit
Default Value: *XXXXXXXXh* ***Power Well:*** Core

Bits	Name	Description	Reset Value	Access
31:00	DTA	**Data:** 32-bit data value that is written to the register pointed to by SIRI, or read from the register pointed to by SIRI.	*XXXXXXXX*h	RW

2. XOR chain tables

Issue: The Intel® 3100 Chipset External Design Specification incorrectly lists pin E26 (SMBALERT#\ GPI[11]) in the wrong XOR chain. The pin should not appear in XOR Chain #3 and should appear in XOR Chain #4 instead. This inaccuracy appears in these places:

- Page 302 of the Intel® 3100 Chipset External Design Specification (Intel Confidential #637583)

Issue: The Intel® 3100 Chipset External Design Specification incorrectly lists the output in XOR chain #4. The correct output is pin F1 (GP[10]). This inaccuracy appears on these pages:

- Page 304 of the Intel® 3100 Chipset External Design Specification (Intel Confidential #637583)

The correct tables for XOR Chain #3 (REQ[4:1]# = 0010) and XOR Chain #4 (REQ[4:1]# = 0011) are printed below.

Table 4. XOR Chain #3 (REQ[4:1]# = 0010)

Order	Name	Ball #	Notes
1	STPCLK#	C22	Top of XOR Chain
2	A20M#	A21	2nd signal in XOR
3	CPUSLP#	D21	
4	INTR	C21	
5	NMI	B22	
6	CPUWRGD/GPO[49]	F22	
7	INIT#	D23	
8	SMI#	B23	
9	IGNNE#	A23	
10	FERR#	A24	
11	THRMTRIP#	B32	
12	INTRUDER#	C28	
13	INTVRMEN	C25	
14	SYS_RESET#	K24	
15	SUSCLK#	C22	
16	WAKE#	E25	
17	GPIO[27]	B28	
18	SUS_STAT#/LPCPD#	H28	
19	GPIO[25]	F27	
20	WL_PU[1]	E28	
21	GPIO[24]	D26	
22	PWRBTN#	F28	
23	RI#	J27	
24	GPI[8]	G27	
25	GPIO[28]	J28	
26	SLP_S3#	D29	
27	SLP_S4#	E29	
28	SLP_S5#	G29	
29	SMBDATA	H29	
30	SMBCLK	G30	30th signal in XOR
31	SMLINK[1]	F30	31nd signal in XOR
32	SMLINK[0]	D30	
33	PME#	P31	
34	PCIRST#	C34	
35	PLTRST#	P32	
Output	GPIO[1]	D35	XOR Chain #3 OUTPUT

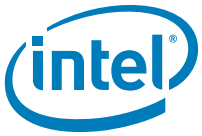


Table 5. XOR Chain #4 (REQ[4:1]# = 0011) (Sheet 1 of 3)

Order	Name	Ball #	Notes
1	SATA_RXn[2]	K17	Top of XOR Chain
2	SATA_RXp[2]	K18	2nd signal in XOR
3	SATA_TXn[2]	L17	
4	SATA_TXp[2}	L16	
5	SATA_RXn[3]	G20	
6	SATA_RXP[3]	G21	
7	SATA_TXn[3]	H20	
8	SATA_TXp[3]	H19	
9	SATA4_GP/ GPI[12]	G18	
10	PIRQ[D]#	C30	
11	SPKR	C33	
12	CLK14	B34	
13	PIRQ[H]#/GPI[5]	E32	
14	PIRQ[G]#/GPI[4]	F31	
15	PIRQ[F]#/GPI[3]	E31	
16	PIRQ[E]#/GPI[2]	D32	
17	PIRQ[A]#	C31	
18	PIRQ[B]#	A30	
19	PIRQ[C]#	B29	
20	GPI[0]	A33	
21	GPO[16]	D36	
22	GPI[1]	D35	
23	N/C	B31	
24	GPO[17]	A32	
25	DEVSEL#	F36	
26	REQ[1]#	E34	
27	GNT[0]#	D33	
28	PERR#	G36	
29	STOP#	G35	
30	AD[27]	G33	
31	N/C	E35	
32	AD[29]	F34	
33	AD[24]	H34	
34	PLOCK#	H35	
35	AD[28]	H32	35th signal in XOR
36	AD[25]	J30	36th signal in XOR
37	REQ[0]#	H31	
38	AD[31]	G32	
39	AD[30]	F33	
40	SERR#	J36	

Table 5. XOR Chain #4 (REQ[4:1]# = 0011) (Sheet 2 of 3)

Order	Name	Ball #	Notes
41	AD[14]	J34	
42	C/BE[3]#	J33	
43	AD[26]	J31	
44	AD[13]	K32	
45	AD[12]	K33	
46	GPI[40]	K30	
47	C/BE[0]#	K29	
48	N/C	L28	
49	AD[7]	L29	
50	AD[15]	K36	
51	PAR	K35	
52	C/BE[1]#	L35	
53	AD[10]	L34	
54	AD[22]	L31	
55	AD[23]	L32	
56	PCICLK	M28	
57	AD[20]	M30	
58	AD[19]	M31	
59	AD[6]	M34	
60	C/BE[2]#	N30	
61	AD[5]	M33	
62	AD[11]	M36	
63	IRDY#	N29	
64	AD[9]	N35	
65	AD[8]	N36	
66	AD[4]	N32	
67	AD[3]	N33	
68	TRDY#	P28	
69	GNT[1]#	P29	
70	GPO[48]	P34	70th signal in XOR
71	N/C	P35	71st signal in XOR
72	AD[17]	R30	
73	AD[21]	R34	
74	FRAME#	T29	
75	AD[2]	R36	
76	AD[18]	U35	
77	AD[0]	T36	
78	AD[1]	T35	
79	AD[16]	T30	
80	PEB_RPC[0]	T33	

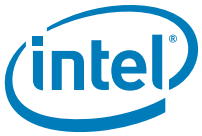


Table 5. XOR Chain #4 (REQ[4:1]# = 0011) (Sheet 3 of 3)

Order	Name	Ball #	Notes
81	N/C	T32	
82	PEB_RPC[1]	R31	
83	WDT_TOUT#	W27	
84	SIU_RXD[1]	V27	
85	SIU_TXD[1]	V35	
86	SIU_CTS[1]#	V36	
87	SIU_DSR[1]#	W35	
88	SIU_DCD[1]#	V34	88th signal in XOR
89	SIU_RI[1]#	V29	89th signal in XOR
90	SIU_DTR[1]#	V26	
91	SIU_RTS[1]#	V31	
92	SIU_RXD[2]	V30	
93	SIU_TXD[2]	V33	
94	SIU_CTS[2]#	W34	
95	SIU_DSR[2]#	W33	
96	SIU_DCD[2]#	V32	
97	SIU_RI[2]#	W28	
98	SIU_DTR[2]#	W29	
99	SIU_RTS[2]#	W32	
100	UART_CLK	W30	
101	N/C	R33	
102	N/C	U31	
103	N/C	U32	
104	N/C	U34	
105	SMBALERT#\ GPI[11]	E26	
Output	GP[10]	F1	XOR Chain #4 OUTPUT

3. Added processor support

Issue: Added support for the following processors:

- Intel® Celeron® M Processor ULV 423 (1.067 GHz)
- Intel® Core™ Duo processor ULV U2500 (1.2 GHz).
- Intel® Celeron® Processor
- Dual-Core Intel® Xeon® Processor LV
- Dual-Core Intel® Xeon® Processor ULV

Affected Docs: Intel® 3100 Chipset External Design Specification, Intel® 3100 Chipset Datasheet, and Intel® Core™ Duo Processor and Intel® 3100 Chipset Platform User Manual.

4. Added L7400 processor support

Issue: Added support for the Intel® Core™2 Duo processor L7400.

Affected Docs: Intel® 3100 Chipset External Design Specification, Intel® 3100 Chipset Datasheet, and Intel® Core™ Duo Processor and Intel® 3100 Chipset Platform User Manual.

5. Added U7500 processor support

Issue: Added support for the Intel® Core™2 Duo processor U7500.

Affected Docs: Intel® Core™2 Duo Processor and Intel® Core™ Duo Processor and Intel® 3100 Chipset CRB User's Manual is updated as follows:

1. Table 4 (Supported Microprocessors) in Section 1.2 is changed to the following.

Microprocessor	Cores	CLK Speed	FSB Speed	L2 Cache	TDP
Intel® Core™2 Duo Processor L7400	Dual	1.50GHz	667MHz	4MB	17W
Intel® Core™2 Duo Processor U7500	Dual	1.06GHz	533MHz	2MB	10W
Intel® Core™ Duo processor ULV U2500	Dual	1.20GHz	533MHz	2MB	9W
Intel® Celeron® M Processor ULV 423	Single	1.06GHz	533MHz	1MB	5.5W

Affected Docs: Intel® Core™ Duo ULV 2500 and Intel® 3100 Chipset Platform Design Guide (PDG) is updated as follows:

2. The title of this PDG is changed to: Intel® Core™2 Duo Processor and Intel® Core™ Duo Processor and Intel® 3100 Chipset Platform Design Guide.
3. All 17 occurrences of (L7400) through-out the PDG get changed to (L7400/U7500).
4. Table 2 (Processor Table) in Section 1.0 is changed to the following.

Brand Name
Intel® Core™2 Duo Processor L7400 (1.5 GHz)
Intel® Core™2 Duo Processor U7500 (1.067 GHz)
Intel® Core™ Duo processor ULV U2500 (1.2 GHz)
Intel® Celeron® M Processor ULV 423 (1.067 GHz)

5. Table 4 (Processor Detail) in Section 2.1.1 is changed to the following.

Processor	Freq. (GHz)	Process (nm)	L1 Cache (I+D)	L2 Cache	FSB (MHz)	Streaming SIMD Extensions2 (SSE2)	Data Prefetch Logic	Package technology	Speed step	Supports IA with Dynamic Execution
L7400	1.5	65	64KB	4MB	667	YES	YES	uFC-BGA	YES	YES
U7500	1.06	65	64KB	2MB	533	YES	YES	uFC-BGA	YES	YES
ULV U2500	1.2	65	64KB	2MB	533	YES	YES	uFC-BGA	YES	YES
ULV 423	1.06	65	64KB	1MB	533	YES	YES	uFC-BGA	NO	YES

Affected Docs: Intel® 3100 Chipset Datasheet is updated as follows:

6. Table 4 (Supported Microprocessors) in Section 1.2 should include all of the following.

Processor	Freq. (GHz)	Process (nm)	L1 Cache (I+D)	L2 Cache	FSB (MHz)	Streaming SIMD Extensions2 (SSE2)	Data Prefetch Logic	Package technology	Speed step	Supports IA with Dynamic Execution
L7400	1.5	65	64KB	4MB	667	YES	YES	uFC-BGA	YES	YES
U7500	1.06	65	64KB	2MB	533	YES	YES	uFC-BGA	YES	YES
ULV U2500	1.2	65	64KB	2MB	533	YES	YES	uFC-BGA	YES	YES
ULV 423	1.06	65	64KB	1MB	533	YES	YES	uFC-BGA	NO	YES

Affected Docs: Intel® 3100 Chipset External Design Specification is updated as follows:

7. Table 1 (Supported Microprocessors) in Section 1.2 is changed to the following.

Microprocessor	FSB Speed	FSB Parity
Intel® Pentium® M Processor 745 (1.8 GHz)	400MHz	NO
Intel® Pentium® M Processor LV 738 (1.4 GHz)	400MHz	NO
Intel® Celeron® M Processor ULV 373 (1.0 GHz)	400MHz	NO
Intel® Celeron® M Processor 370 (1.5 GHz)	400MHz	NO
Intel® Celeron Processor (1.66 GHz)	667MHz	YES
Dual-Core Intel® Xeon® Processor LV (2.0 GHz, 1.66 GHz)	667MHz	YES
Dual-Core Intel® Xeon® Processor ULV (1.66 GHz)	667MHz	YES
Intel® Core™2 Duo Processor L7400 (1.5 GHz)	667MHz	NO
Intel® Core™2 Duo Processor U7500 (1.067 GHz)	533MHz	NO
Intel® Core™ Duo processor ULV U2500 (1.2 GHz)	533MHz	NO
Intel® Celeron® M Processor ULV 423 (1.067 GHz)	533MHz	NO

6. USB3/2 ports need to be swapped in User's Manuals

Issue: The physical location reference of both USB3 and USB2 Ports need to be swapped in two of the three published Intel 3100 Chipset-based Development Kit User's Manuals, per the following fixes:

FROM:

- USB ports (2) 2 top / 3 bottom per Table 3 Component Layout Description
- USB ports (2) 2 top / 3 bottom per Figure 30 Back Panel Connectors

TO:

- USB ports (2) 3 top / 2 bottom per Table 3 Component Layout Description
- USB ports (2) 3 top / 2 bottom per Figure 30 Back Panel Connectors

Affected Docs: Intel® Pentium® M Processor on 90 nm Process and Intel® 3100 Chipset Development Kit User's Manual (Jan. 2007) and Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Development Kit User's Manual (Jan. 2007)

7. Miscellaneous CAP and RES typos and clarifications

Issue: There are several typos and clarifications common to all three Intel 3100 Chipset Platform Design Guides that require the following fixes:

All Sections 19.6.14 titled "FWH Decoupling"

- FROM 0.4.7 µF capacitor TO 4.7 µF capacitor.

All Tables titled "Intel 3100 Chipset Schematic Checklist"

- For SERIRQ signal, add a tolerance of +/- 5% to the 8.2 - 10K ohm resistor
- For RTEST# signal, delete the "ohm' notation after the 1.0 uF capacitor
- For INTRUDER# signal, add a tolerance of +/- 5% to the 1M ohm resistor
- For all GPIO signals, add a tolerance of +/- 5% to every 10K ohm resistor

Affected Docs: Intel® Pentium® M Processor on 90nm process and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), Dual-Core Intel® Xeon® Processor LV and Intel® 3100

Chipset Platform Design Guide (Jan. 2007), and Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

8. INIT3_3V# addition to chipset checklist

Issue: INIT3_3V# is a Intel 3100 Chipset signal and not a Processor signal. Therefore, the table entry for INIT3_3V# is deleted from Processor Schematic Checklist Table and is added to the Intel 3100 Chipset Schematic Checklist Table within the Firmware Hub/ LPC Interface section. This fix applies to all three Intel 3100 Chipset Platform Design Guides and is specific to the following checklist recommendation:

- INIT3_3V# Connect to FWH. Pull-up using 4.7K ohm +/- 5% resistor.

Affected Docs: Table 92 and 93 in the Intel® Pentium® M Processor on 90nm process and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), and Table 93 and 94 in the Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), and Table 95 and 96 in the Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

9. PDF page numbers should match Adobe* Reader*

Issue: There are either missing or duplicate page numbers within all three published Intel 3100 Chipset Platform Design Guides, causing all higher page numbers to be offset by 1 page as displayed within the Adobe* Reader* toolbar while navigating through the document. All page number issues are identified in the Affected Docs section (below) and will be fixed during the next revision update cycle for all Intel 3100 Chipset Platform Design Guides.

Affected Docs: Page 123 does not exist in the Intel® Pentium® M Processor on 90nm process and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), Page 127 exists twice in the Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), and Page 112 exists twice in the Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)

10. VREF tolerance fixed to +/-2%

Issue: The VREF 0.1% tolerance recommendation per Power Deliver Layout Checklist Tables in all three Intel 3100 Chipset Platform Design Guides is a typo and conflicts with the required VREF +/- 2% specification per Intel 3100 Chipset Datasheet. The following fix is required:

FROM: A VREF tolerance of 0.1% is required

TO: A VREF tolerance of +/- 2% is required

Affected Docs: Table 103 in the Intel® Pentium® M Processor on 90nm process and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), and Table 104 in the Dual-Core Intel® Xeon® Processor LV and Intel® 3100 Chipset Platform Design Guide (Jan. 2007), and Table 106 in the Intel® Core™ Duo Processor ULV U2500 and Intel® 3100 Chipset Platform Design Guide (Jan. 2007)